REMARKS

No claims have been canceled or amended. Claims 1-20 remain pending in the captioned case. Further examination and reconsideration of the captioned application is respectfully requested.

Allowed and Allowable Subject Matter

Applicants appreciate the Examiner's indication that claims 9-20 are allowed. In addition, it has been indicated that claim 8 contains allowable subject matter. Applicants acknowledge these claims are patentably distinct over the cited art. However, Applicants believe that rejected claims 1-7 also contain allowable subject matter, and are patentably distinct over the cited art as described in more detail below.

Section 102 Rejection

Claims 1, 2, and 4-7 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,507,213 to Dangat (hereinafter "Dangat"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d. 1051, 1053 (Fed. Cir. 1987); MPEP 2131. Dangat does not disclose each and every element of the currently pending claims, either inherently or expressly, some distinctive features of which are set forth in more detail below.

Dangat does not teach or suggest multiple integrated circuits, each having a plurality of input pins. Present claim 1 is the only rejected independent claim. Claim 1 specifically recites, in the first element, multiple integrated circuits. Claim 1 also recites a plurality of input pins for each of the multiple integrated circuits. Although Applicants do not believe the term "integrated circuit" need be defined to one of skill in the art or otherwise; nonetheless, definitions of "integrated circuit" are available in numerous treatises. For example, the New IEEE Standard Dictionary of Electrical and Electronic Terms (5th Ed. 1993), page 662, defines "integrated circuit" as a "combination of interconnected circuit elements inseparably associated with or within a continuous substrate." Typically, an integrated circuit is embodied on a silicon or gallium arsenide substrate, with dopants placed into the substrate active areas and overlying thin films used to form the interconnection of circuit elements prior to dicing separate die or chips from a wafer. The integrated circuit, die, or chip separated from the wafer can then be packaged and placed on, for

example, a printed circuit board. The packaged integrated circuits can then be interconnected by trace conductors on the printed circuit board to form an interconnection of multiple integrated circuits.

Contrary to claim 1 reciting multiple integrated circuits, each having a plurality of input pins, Dangat recites a plurality of configuration blocks 118 arranged upon a singular (not multiple) integrated circuit 100 (Dangat -- Fig. 2). In particular, Dangat states that circuit 100 comprises a PLD and memory 102, which may each be implemented "on a separate die." (Dangat -- col. 2, lines 41-43; col. 2, lines 54-55.) Thus, the PLD circuit 100 which encompasses the parallel-coupled configuration blocks 118 in Dangat is a singular integrated circuit (Dangat -- col. 3, lines 39-42), separate and apart from the integrated circuit which bears memory 102. Moreover, even assuming hypothetically that configuration blocks 118 in Dangat can be embodied on separate substrates to form multiple integrated circuits, each configuration block has a single input pin 122 -- certainly not the same as the claimed plurality of input pins associated with each of the multiple integrated circuits, as set forth in claim 1.

Dangat does not teach or suggest a single access port that selectively places a parallel delivered signal onto the plurality of input pins of each of said multiple integrated circuits. Present independent claim 1 recites a single access port that not only receives a serial bitstream, but converts the serial bitstream into the parallel delivered signal placed onto the plurality of input pins for each of the multiple integrated circuits. For example, single access port 46 can receive a serial bitstream across TDI and convert the serial bitstream into parallel delivered signals to core 50a, core 50b, etc. of integrated circuits 48a, 48b, etc. (Specification -- Fig. 3; pg. 6, lines 9-24; pg. 9, line 22- pg. 10, line 14). Present Fig. 3 illustrates that in addition to two integrated circuits 48a and 48b, many other integrated circuits can have a plurality of input pins for receiving the parallel delivered signal from port 46. *See*, Fig. 3 -- the ellipsis appended to series of integrated circuits 48. Thus, while controller 46 might reside on one integrated circuit, the output from controller 46 is forwarded into a plurality of pins on many integrated circuits.

Contrary to present claim 1, Dangat does not suggest a single access port that feeds a plurality of input pins associated with each of multiple integrated circuits. Instead, Dangat illustrates what hypothetically might be construed as an access port 106 that only feeds a single integrated circuit 100 (Dangat -- Fig. 2). Alternatively, if distribution logic 114 is construed as an access port, then while it receives a serial bitstream 120, distribution logic 114 does not present a parallel delivered signal to a plurality of input pins associated with each of multiple integrated circuits, since block 116 of Dangat is

construed to be on the same integrated circuit 100 as distribution logic 114 (Dangat – col. 2, lines 41-43; col. 2, lines 54-57).

For at least the reasons stated above, Applicants assert that independent claim 1 and claims dependent therefrom are not anticipated by the cited art. Accordingly, Applicants respectfully request removal of this rejection.

Section 103 Rejection

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Dangat in view of U.S. Patent No. 6,512,394 to Lacey et al. (hereinafter "Lacey"). For at least the reasons cited above in response to the § 102 rejection, Applicants assert that dependent claim 3 is patentable over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

CONCLUSION

The present response is believed to be a complete response to the issues raised in the Office Action mailed April 13, 2004. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-20 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-06200.

Respectfully submitted,

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